Name: \_\_\_\_\_Dillon Britt\_\_\_\_

**CPHE 222 Organization, Architecture, and Assembly Language  
Chapter #5A Reading Quiz**

This is a take-home reading quiz. Your textbooks is the only outside resource that you are allowed to use while completing this quiz. Do NOT consult with other students or anyone else while working on this quiz. Answer each question below based on the material in the reading assignment (Chapter 5.1-5.3).

# Chapter 5A

1. The principle of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ locality states that if memory location is accessed once, it will tend to be accessed again soon. (5.1)

**Temporal**

1. The principle of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ locality states that if memory location is accessed once, other memory locations whose addresses are close by will tend to be accessed soon. (5.1)

**Spatial**

1. In a typical memory hierarchy, memories close to processor are typically <faster, slower>, <smaller, larger>, and <cheaper, more expensive> than memories farther from the processor. (Circle one in each pair.) (5.1)
2. Although modern processors do not always implement memory hierarchies this way, for this class we will assume that data is hierarchical – a level closer to the processor contains a \_\_\_\_\_\_\_\_\_\_ of the previous memory. (5.1)

**Block**

1. Due to spatial locality, we never transfer just a single byte/word of data between levels of memory. The minimum amount of data that is transferred/processed in a hierarchical memory is called a \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. (5.1)

**Block**

1. Match the following definitions with the keywords given below. Write the letter of the matching word in the space provided. (5.1)

\_\_D\_\_ The ratio of memory accesses not found in a level of memory to the total number of memory accesses made.

\_\_A\_\_ The term used to describe finding the needed memory location in a particular level of memory.

\_\_F\_\_ The time required to access a level of memory including the time needed to determine whether or not an access is a hit or miss.

\_\_B\_\_ The term used to describe failing to find the needed memory location in a particular level of memory.

\_\_E\_\_ The time required to fetch a block of memory from a lower memory level.

\_\_C\_\_ The ratio of memory accesses found in a level of memory to the total number of memory accesses made.

*Keywords:* (A) Hit (B) Miss (C) Hit rate (D) Miss rate (E) Hit time (F) Miss penalty

1. For each statement below, identify it as true for SRAM, DRAM, or both by placing checkmarks in the correct column(s). (5.2)

|  |  |  |
| --- | --- | --- |
| SRAM | DRAM |  |
|  |  | Has a fixed access time (although the read time and write time can be different). |
|  |  | Is considered “volatile” memory. |
|  |  | Each memory bit is stored using 6-8 transistors. |
|  |  | Each memory bit is stored using 1 transistor + 1 capacitor. |
|  |  | Memory values have to be refreshed every few milliseconds or they would vanish. |
|  |  | Memory values can be maintained with minimal power. |
|  |  | Has a higher memory bit density and therefore can be built more cheaply. |

1. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ is the process of remapping Flash memory blocks that have been written many times to less used blocks. (5.2)

**EEPROM**

1. In traditional magnetic disk hard drives, data is stored on \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ circles or tracks. (5.2)

**Concentric**

1. In traditional magnetic disks, accessing data is a three-stage process. List the stages below. (5.2)
   1. seek
   2. Rotational Latency
   3. Transfer time
2. Average rotational latency is dependent on what hard drive characteristic that can verify between hard drive models? (5.2)

**Round Per minute**

1. The levels of memory between the processor and main memory are called \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. (5.3)

**Cache**

1. A cache structure that uses a many-to-one mapping scheme is called a \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ cache. (5.3)

**Direct Mapped**

1. What four fields are present in each row of a direct-mapped cache? (5.3)
   1. Index
   2. v
   3. Tag
   4. Data
2. There are various cache schemes used for writing data to a cache. In the \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ scheme, data is only written to the cache at the time of a write (store word) and written back to main memory only when that particular block of data is replaced in the cache. (5.3)

**Write Through**

|  |  |
| --- | --- |
| **Cache** | |
| Index | Data |
| 00 |  |
| 01 |  |
| 10 |  |
| 11 |  |

1. There are various cache schemes used for writing data to a cache. In the \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ scheme, data is written to all cache levels and main memory at the time of the write (store word). (5.3)

**Write Buffer**

1. For the memory and direct-mapped cache shown below, draw arrows from every memory location highlighted in blue to the specific cache location in which that block of data can be written. (5.3)

|  |  |
| --- | --- |
| **Memory** | |
| Address | Data |
| 0000 0000 |  |
| 0000 0001 |  |
| 0000 0010 |  |
| 0000 0011 |  |
| 0000 0100 |  |
| 0000 0101 |  |
| 0000 0110 |  |
| 0000 0111 |  |
| 0000 1000 |  |
| 0000 1001 |  |
| 0000 1010 |  |
| 0000 1011 |  |
| 0000 1100 |  |
| 0000 1101 |  |
| 0000 1110 |  |
| 0000 1111 |  |
| 0001 0000 |  |
| 0001 0001 |  |
| 0001 0010 |  |
| 0001 0011 |  |